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WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second spaced-apart doped region formed in the surface;

a third doped region over said first doped region and of a different conductivity type than said first doped region;

a fourth doped region over said second doped region and of a different conductivity type than said second doped region;

a first oxide layer of a first predetermined thickness proximate said third doped region; and

a second oxide layer of a second predetermined thickness proximate said fourth doped region.

2. The integrated circuit structure of claim 1 wherein the first doped region is a first source/drain region of a first MOSFET and the third doped region is a channel region of the first MOSFET.

3. The integrated circuit structure of claim 1 wherein the third doped region is a first source/drain region of a second MOSFET and the fourth doped region is a channel region of the second MOSFET.

4. The integrated circuit structure of claim 3 wherein the first and the second MOSFETs have a different threshold voltage.

5. The integrated circuit structure of claim 1 further comprising:

a fifth doped region over the third doped region of a different conductivity type than the third doped region, wherein said fifth doped region is a second source/drain region of a first MOSFET;

a sixth doped region over the fourth doped region of a different conductivity type than the fourth doped region, wherein said sixth doped region is a second source/drain region of a second MOSFET; and

wherein said first and said second MOSFETs have different threshold voltages.

6. The integrated circuit structure of claim 5 further comprising a first gate contact in electrical communication with the first oxide layer, forming a gate of the first MOSFET, and a second gate contact in electrical communication with the second oxide

layer, forming a gate of the second MOSFET, and wherein the first and the second MOSFETs can withstand different gate input voltages as a consequence of the differing gate oxide thickness.

7. The integrated circuit structure of claim 5 wherein the first oxide layer is a gate oxide layer of the first MOSFET, and wherein the second oxide layer is a gate oxide layer of the second MOSFET, and wherein the first and the second MOSFETs have a different threshold voltage.

8. The integrated circuit structure of claim 1 wherein the first and second doped regions are first and second source/drain regions, and wherein the third and the fourth doped regions are channel regions, the integrated circuit structure further comprising:

a fifth and a sixth spaced-apart source/drain region each vertically aligned with one of the third and fourth doped regions, wherein said fifth and said sixth doped regions are of a conductivity type opposite to the adjacent third and fourth doped regions, respectively;

wherein the first, third, and fifth doped regions form a first transistor, and wherein the second, fourth, and sixth doped regions form a second transistor;

a first and a second conductive element adjacent the first and the second oxide layers, respectively, to control operation of the respective first and second transistor; and

wherein the breakdown voltage of the first and the second MOSFETs is related to the first oxide layer thickness and the second oxide layer thickness, respectively.

9. The integrated circuit structure of claim 8 wherein the first and the second conductive elements comprise polysilicon and serve as the gate for the first and the second transistors, respectively.

10. An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second spaced-apart doped region formed on said major surface;

a third doped region overlying said first doped region and of a different conductivity type than said first doped region;

a first oxide layer of a first predetermined thickness proximate said third doped region;

a conductive layer formed between said first and said second doped regions and above said major surface, providing electrical connection between said first and said second doped regions;

a fourth and a fifth spaced-apart doped region formed in said major surface;

a sixth doped region overlying said fourth doped region and have a different conductivity type than said fourth doped region;

a second oxide layer of a second predetermined thickness proximate said sixth doped region; and

a conductive layer formed between said fourth and said fifth doped regions and above said major surface, providing electrical connection between said firth and said sixth doped regions.

11. The integrated circuit structure of claim 10

wherein the first doped region is a source/drain region of a first MOSFET and the third doped region is a channel region of said first MOSFET;

wherein the second doped region is a source/drain region of a second MOSFET, said structure further comprising a channel region of said second MOSFET aligned with the source/drain region of said second MOSFET;

wherein the fourth doped region is a source/drain region of a third MOSFET and the sixth doped region is a channel region of said third MOSFET;

wherein the fifth doped region is a source/drain region of a fourth MOSFET, said structure further comprising a channel region of said fourth MOSFET aligned with said source/drain region of said fourth MOSFET.

12. The integrated circuit structure of claim 11 wherein the first and the second MOSFETs are of a complimentary conductivity type, and wherein the third and the fourth MOSFETs are of a complimentary conductivity type.

13. The integrated circuit structure of claim 11 wherein the first and the second MOSFETs are configured to form a first inverter circuit and wherein the third and the fourth MOSFETs are configured to form a second inverter circuit.

14. The integrated circuit structure of claim 11 wherein each one of the first and the second MOSFETs has a gate oxide thickness sized to accommodate a first input

voltage, and wherein each one of the third and the fourth MOSFETs has a gate oxide thickness sized to accommodate a second input voltage.

15. An integrated structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second doped source/drain region formed in the major surface;

a first channel region overlying said first source/drain region and having a different conductivity type than said first source/drain region;

a second doped channel region overlying said second source/drain region and having a different conductivity type than said second source/drain region;

a third and a fourth doped spaced-apart source/drain region, wherein said third source/drain region is vertically aligned with said first channel region and said first source/drain region, and wherein said fourth source/drain region is vertically aligned with said second source/drain region and said second channel;

a first and a second oxide layer of a first predetermined thickness proximate to, respectively, said first and said second channel regions;

a fifth and a sixth doped space-apart source/drain region formed in the major surface;

a third channel region formed over said fifth source/drain region;

a fourth channel region formed over said sixth source/drain region;

a seventh and an eighth doped spaced-apart source/drain region, wherein said seventh source/drain region is vertically aligned with said third channel region and said fifth source/drain region, and wherein said eighth source/drain region is vertically aligned with said sixth source/drain region and said fourth channel region;

a third and a fourth oxide layer each having a second predetermined thickness proximate, respectively, said third and said fourth channel regions;

a first conductive element connected to said first and said second channel regions to control operations thereof; and

a second conductive element connected to said third and said fourth channel regions to simultaneously control operation thereof.

16. The structure of claim 15 wherein the first and the second conductive elements each comprise polysilicon.

17. The integrated circuit structure of claim 15 wherein a first MOSFET comprises the first and the third source/drain regions and a first gate further comprising the first channel region and the first oxide layer, and wherein a second MOSFET comprises the second and the fourth source/drain regions and a second gate further comprising the second channel region and the second oxide layer, and wherein a third MOSFET device comprises the fifth and the seventh source/drain regions and a third gate further comprising the third channel region and the third gate oxide, and wherein a fourth MOSFET device comprises the sixth and the eighth source/drain regions and a fourth gate further comprising the fourth channel region and the fourth oxide layer, and wherein said first and said second MOSFETs form a first complimentary MOSFET device, and wherein the first and the second predetermined oxide layer thickness accommodates, without breakdown, a first input voltage for said first complimentary MOSFET device, and wherein said third and said fourth MOSFETs form a complimentary MOSFET device, and wherein the third and the fourth predetermined oxide layer thickness accommodates, without breakdown, a second input voltage for said second complimentary device.

18. An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second spaced-apart doped region formed on said major surface;

a third doped region overlying said first doped region and of a different conductivity type than said first doped region;

a first oxide layer of a first predetermined thickness proximate said third doped region;

a conductive layer interconnecting said first and said second doped regions;

a fourth doped region overlying said second doped region and having a different conductivity type than said second doped region;

a second oxide layer of a second predetermined thickness proximate said fourth doped region;

a fifth doped region overlying said third doped region;

a sixth doped region overlying said fourth doped region; and

a conductive layer providing electrical connection between said fifth and said sixth doped regions.

19. The integrated circuit structure of claim 18, wherein the first, third and fifth doped regions form a first MOSFET, and wherein said second, fourth and sixth doped regions form a second MOSFET, and wherein said first and said second MOSFETs are electrically connected in parallel, and wherein each of said first and said second MOSFETs has a different gate turn-on voltage related to the thickness of the first and the second oxide layers associated with said first and said second MOSFETs, respectively.

20. A method for fabricating a semiconductor device with a plurality of field-effect transistors comprising:

forming a first device region, selected from the group consisting of a source region and a drain region, of a first field-effect transistor on a semiconductor layer;

forming a second device region, selected from the group consisting of a source region and a drain region, of a second field-effect transistor on said semiconductor layer;

forming a gate for said first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness; and

forming a gate for said second field-effect transistor, wherein said gate has a second predetermined gate oxide thickness.

21. The method of claim 20 including the additional step of configuring the first and the second device regions, and the first and the second gate regions into a circuit comprising two MOSFETs.

22. The method of claim 20 wherein the step of forming the gate having the first predetermined gate oxide thickness and the step of forming the gate having the second predetermined gate oxide thickness, comprises:

forming a gate for the first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

forming a gate for the second field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

removing the oxide from said gate of the first field-effect transistor;

forming gate oxide material on said gate for said first field-effect transistor;

forming gate oxide material on said gate for said second field-effect transistor; and

such that the gate oxide of the first field-effect transistor has a thickness less than the thickness of the gate oxide for the second field-effect transistor.

23. The method of claim 20 wherein the first and the second field-effects transistors can withstand different gate input voltages as a consequence of the differing predetermined gate oxide thickness.

24. A method for fabricating a semiconductor device with a plurality of transistors comprising:

forming first and second spaced-apart diffusion regions on a semiconductor layer;

forming a third semiconductor region over said first diffusion region, wherein said third semiconductor region has an opposite conductivity type than said first diffusion region;

forming a fourth semiconductor region over said second diffusion region wherein said fourth semiconductor region has an opposite conductivity type than said second diffusion region;

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

forming a second gate oxide of a second predetermined thickness adjacent said fourth semiconductor region;

forming fifth and sixth semiconductor regions, each positioned over one of said third and said fourth semiconductor regions, such that said third and said fifth regions are vertically aligned with one of said first and said second regions, and such that said fourth and said sixth regions are vertically aligned with the other of said first and second regions, the resulting structure providing two transistors.

25. The method of claim 24 wherein the step of forming the first gate oxide of a first predetermined thickness adjacent the third semiconductor region and the step of forming the second gate oxide of the second predetermined thickness adjacent the fourth semiconductor region comprises:

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

forming a second gate oxide of said first predetermined thickness adjacent said fourth semiconductor region;

removing said first gate oxide;

forming a third gate oxide of a second predetermined thickness adjacent said third semiconductor region;

forming said third gate oxide of said third predetermined thickness adjacent said fourth semiconductor region; and

wherein the gate oxide thickness adjacent said fourth semiconductor region is the sum of said first predetermined thickness plus said second predetermined thickness.

26. The method of claim 24 wherein the first and the second gate oxides are associated with a first and a second MOSFET, and wherein said first and said second MOSFETs form a complimentary MOSFET device, and wherein said third and said fourth gates are associated with a third and a fourth MOSFET, respectively, and wherein said third and said fourth MOSFETs form a second complimentary MOSFET device; and wherein the gate terminals of said first complimentary MOSFET device have a first breakdown voltage related to the first predetermined thickness, and wherein the gate terminals of said second MOSFET device have a second breakdown voltage related to the second predetermined thickness.